Pinouts for selected TTL Chips The following diagrams provide pinout information for selected TTL chips. For more complete information about the behavior of each chip and information on other chips, see the “TTL Logic” manual in the Lab.

### Functional Index

This index only includes the selected chips that appear on the following pages. For a complete functional index, see the “TTL Logic” manual in the lab. The entries in the O column in the following tables indicate the type of output the gate has. ▽ indicates that the gate has tri-state outputs, ▷ indicates that the gate has open-collector outputs, and a blank indicates that the gate has standard two level logic outputs.

<table>
<thead>
<tr>
<th>Description</th>
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<tr>
<td>Hex Inverters</td>
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<tr>
<td>Hex Inverters</td>
<td>▷</td>
<td>'05</td>
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<td>Quad 2-Input Gates</td>
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<tr>
<td>Triple 3-Input Gates</td>
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<td>Dual 4-Input Gates</td>
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<tr>
<td>Hex Inverter</td>
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- **Flip-Flops, Registers and Latches**

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<tr>
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<td>Dual JK Pulse Triggered</td>
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<td>Octal D Edge Triggered</td>
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<td>Octal D Transparent</td>
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- **Asynchronous (Ripple) Counters - Negative Edge Triggered**

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<td>Decade</td>
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<tr>
<td>4 Bit Binary</td>
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- **Data Selectors / Multiplexers**

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- **Decoders / Demultiplexers**

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<tr>
<td>3 to 8</td>
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<tr>
<td>BCD to Decimal</td>
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<tr>
<td>4 to 16</td>
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- **Arithmetic Operators**

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<tr>
<td>Quad Exclusive Or/Nor</td>
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00 Quadruple 2-Input Positive Logic Nand Gates
\[ Y = \overline{A \cdot B} \]

Vcc: (14)  
Gnd: (7)

02 Quadruple 2-Input Positive Logic Nor Gates
\[ Y = \overline{A + B} \]

Vcc: (14)  
Gnd: (7)

03 Quadruple 2-Input Positive Logic Nand Gates with Open Collector Outputs
\[ Y = \overline{A \cdot B} \]

Vcc: (14)  
Gnd: (7)

04 Hex Inverters
\[ Y = \overline{A} \]

Vcc: (14)  
Gnd: (7)

05 Hex Inverters with Open Collector Outputs
\[ Y = \overline{A} \]

Vcc: (14)  
Gnd: (7)

06 Hex Inverter Buffer/Divers with High Voltage Open Collector Outputs
\[ Y = \overline{A} \]

Vcc: (14)  
Gnd: (7)

07 Hex Buffer/Divers with High Voltage Open Collector Outputs
\[ Y = A \]

Vcc: (14)  
Gnd: (7)
08 Quadruple 2-Input Positive Logic And Gates

1A \( \overline{1} \)
1B \( 1 \)
2A \( 2 \)
2B \( 4 \)
3A \( 9 \)
3B \( 12 \)
4A \( 13 \)
4B \( \overline{1} \)

Vcc: (14) Y = AB
Gnd: (7)

10 Triple 3-Input Positive Logic Nand Gates

1A \( \overline{1} \)
1B \( 1 \)
1C \( 1 \)
2A \( 2 \)
2B \( 4 \)
2C \( 5 \)
3A \( 9 \)
3B \( 10 \)
3C \( 11 \)

Vcc: (14) Y = ABC
Gnd: (7)

11 Triple 3-Input Positive Logic And Gates

1A \( \overline{1} \)
1B \( 1 \)
1C \( 1 \)
2A \( 2 \)
2B \( 4 \)
2C \( 5 \)
3A \( 9 \)
3B \( 10 \)
3C \( 11 \)

Vcc: (14) Y = ABC
Gnd: (7)

20 Dual 4-Input Positive Logic Nand Gates

1A \( \overline{1} \)
1B \( 1 \)
1C \( 1 \)
1D \( 9 \)
2A \( 2 \)
2B \( 4 \)
2C \( 5 \)
2D \( 13 \)

Vcc: (14) Y = ABCD
Gnd: (7)

21 Dual 4-Input Positive Logic And Gates

1A \( \overline{1} \)
1B \( 1 \)
1C \( 1 \)
1D \( 9 \)
2A \( 2 \)
2B \( 4 \)
2C \( 5 \)
2D \( 13 \)

Vcc: (14) Y = ABCD
Gnd: (7)

25 Dual 4-Input Positive Logic Nor Gates with strobe

1G \( \overline{1} \)
1A \( 1 \)
1B \( 1 \)
1C \( 1 \)
1D \( 9 \)
2G \( 11 \)
2A \( 2 \)
2B \( 4 \)
2C \( 5 \)

Vcc: (14) Y = G(A+B+C+D)
Gnd: (7)
27 Triple 3-Input Positive Logic Nor Gates
\[ Y = A + B + C \]

30 8-Input Positive Logic Nand Gate
\[ Y = ABCDEFGH \]

32 Quadruple 2-Input Positive Logic Or Gates
\[ Y = A + B \]

42 4 Line to 10 Line Decoder (BCD to Decimal)

74 Dual D Positive Edge Triggered Flip-Flops with Preset and Clear

76 Dual JK Master-Slave Flip-Flops with Preset and Clear
76A Dual JK Negative Edge-Triggered Flip-Flops with Preset and Clear

Vcc: (5)  Gnd: (10)

90 Decade Counter

Vcc: (5)  Gnd: (10)

135 Quad Exclusive Or/Nor Gates

Vcc: (16)  Y = A ⊕ B ⊕ C  Gnd: (8)

86 Quadruple 2-Input Positive Logic Exclusive-Or Gates

Vcc: (14)  Y = A ⊕ B  Gnd: (7)

93 4-Bit Binary Counter

Vcc: (5)  Gnd: (10)

138 3 to 8 Decoder/Demultiplexer

Vcc: (16)  Gnd: (8)
175 Quad D Flip-Flops

373 Octal D Latches

374 Octal D Flip-Flops