Photodiode Peripheral Utilization Effect on CMOS APS Pixel Performance
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Abstract—A photodiode (PD)-type CMOS active pixel sensor (APS) pixel is comprised of a reverse-biased PN-junction diode (PD) for photon conversion and charge storage, and a number of MOS transistors. Junction capacitance of the PD has two major components: bottom plate (area) and side wall (periphery). Both play important roles in the electro-optical performance of PD-APS pixels. This paper reports PD peripheral junction utilization effects on the pixel’s electro-optical performance, full-well capacity and spectral response for an 18 μm × 18 μm CMOS PD-APS pixel were improved by opening multiple circular holes in the PD diffusion layer. A prototype CMOS APS imager was designed, fabricated, and tested in 0.5-μm, 5 V, 2P3M CMOS process, containing a 424 × 424 pixel array with smaller sub-arrays for multiple pixel designs. Four test pixels with 7, 11, 14, and 17 circular, 1.6-μm-diameter holes were placed on one pixel array, with one control pixel for reference. Pixel characteristics, dark current, PD capacitance, quantum efficiency, sensitivity, and pixel full-well capacity were measured. It was found that increased PD junction peripheral would potentially help to improve total capacitance of the PD, with the expense of higher dark current. We also found that increased PD peripheral capacitance improves spectral response up to 12% of the PD-APS pixel, especially at short wavelengths.

Index Terms—CMOS image sensors, image sensors, sensitivity.

I. INTRODUCTION

CHARGE-COUPLED device (CCD) technology has been leading the field of solid-state imaging for over two decades, in terms of production yield and performance. In the early 1990s, a relatively new image sensor technology called active pixel sensor (APS) [1], manufacturable using existing CMOS facilities and processes, has emerged as a potential CCD replacement. While CMOS APS technology was originally considered inferior, continuous improvements in cost, power consumption [2], dynamic range [3], blooming threshold, readout scheme and speed [4], low supply voltage operation [2], large array size [5], radiation hardness [6], and smartness have achieved performance equal to or better than CCD technology [7], [8].

Electro-optical performance of a photodiode (PD) type APS pixel is directly related to certain physical properties of PD diffusion. Doping concentration, junction depth, junction grading, biasing conditions, and physical shape of the PD diffusion layer determine the pixel full-well capacity, which is one of the main performance benchmarks of the PD-APS pixel. Pixel full-well capacity, along with the biasing condition, is related to sensitivity, charge capacity, charge saturation, dynamic range, noise performance, and the spectral response of the pixel, [9].

The first section of this paper discusses identification of junction and circuit parasitics and their use in improving the full-well capacity of a three-transistor (3T) PD-APS pixel through PD peripheral capacitance utilization. This method also helps to improve spectral response of PD-APS pixels by improving the lateral collection efficiency of the PD junction, as discussed in the paper’s second section. We evaluated this method, and its proposed benefits, by designing a multiple-test-pixel PD-APS imager in a 0.5-μm 5-V 2P3M CMOS process, discussed in sections three and four, with measurement results and discussions in sections five and six, respectively.

II. PD PERIPHERAL UTILIZATION METHOD

The theory behind the PD peripheral utilization method (PPUM) is that, if the pixel pitch is restricted to a certain size, then pixel full-well capacity could be increased by opening holes in the PD’s diffusion area. These diffusion holes could be used to increase PD parasitic capacitance, by increasing the perimeter capacitance of the PD region in certain process technologies. Diffusion holes also can improve spectral response through the lateral collection of charges converted close to the PD’s edges.

A reverse-biased PN-junction diode is used in PD type CMOS APS pixels as a photon conversion and charge (electron) storage element. The total capacitance of the PD diffusion layer determines key pixel performance parameters. For example, wide-dynamic-range pixels require large pixel full-well capacity and low readout noise. PD full-well capacity is comprised of two components: bottom plate (area) and side wall (peripheral) junction parasitic capacitance. Design controls the size of the PD diffusion bottom plate, while peripheral junction depth and doping concentration are process and technology dependent. The PD’s unit area junction capacitance (C_A) and unit peripheral junction capacitance (C_P) are given in the following equations, [9], including technology and design parameters, for the first-order capacitance that contributes to total well capacity

\[ C_{PD} = \frac{C_A \cdot A + C_P \cdot P}{1 - \frac{V_{PD}}{V_{ID}}} \]  

\[ C_{PD} = \frac{C_{3O4A} \cdot A}{1 - \frac{V_{PD}}{V_{EB}}} + \frac{C_{RESW} \cdot P}{1 - \frac{V_{PD}}{V_{RESW}}} \]  

where
C_A, C_P  unit area junction capacitance and unit peripheral junction capacitances, respectively;
C_{JOA}, C_{JOW}  unit zero-bias area and peripheral junction capacitances, respectively;
A, P  area and peripheral of the PD regions, respectively;
\Phi_{DB}, \Phi_{DBW}  built-in potential of area and side-wall junctions, respectively;
M_J, M_{JW}  junction grading coefficients of area and side-wall junctions, respectively;
V_{PD}  PD junction voltage.

Other parasitic capacitances due to the reset and readout transistors in pixel contributing to total PD junction capacitance are shown in Fig. 1 for a three-transistor (3T) PD-APS pixel. These parasitic capacitances contribute to total pixel capacitance differently in different modes of pixel operation, [10]. Right after PD reset and during scene integration periods, overlap capacitances C_{O1} and C_{O2} and gate-to-body capacitance of the readout transistor M2 (C_{T2}) add to the total PD capacitance. During a readout period, Miller capacitance C_{M2} and overlap capacitances C_{O1} and C_{O2} contribute to the total PD capacitance. Contribution of pixel circuit parasitic capacitances is described by the following equations during imaging (3) and readout (4):

\[ C_{\text{par,imaging}} = \left[ W_1 \cdot L_{OL1} + W_2 \cdot \left( L_2 - L_{OL2} \right) \right] \cdot C_{OX} \]  
\[ C_{\text{par,read}} = \left[ \frac{2}{3} \cdot W_2 \cdot \left( L_2 - 2 \cdot L_{OL2} \right) \cdot [1 - G] \right] \cdot C_{OX} + \left[ W_1 \cdot L_{OL1} + W_2 \cdot L_{OL2} \cdot [2 - G] \right] \cdot C_{OX} \]  

where

\[ W_1, W_2 \]  channel width of the reset and source-follower transistors, respectively;
\[ L_{OL1}, L_{OL2} \]  channel overlap length of the reset and source-follower transistors, respectively;
\[ C_{OX} \]  unit oxide capacitance;
\[ G \]  pixel source follower gain factor.

C_A and C_P of a few CMOS process technologies, with minimum feature sizes 2.0 \mu m to 0.18 \mu m, is shown in Fig. 2 [10]. Unit-area capacitance is larger for deep sub-micron devices with a minimum feature size < 0.5 \mu m, due to the increased channel-stop doping-level (for better device isolation, higher diffusion doping concentrations, and shallower junction depths) [11]. Thus, peripheral junction capacitance could be better utilized in processes that have equal or more unit peripheral junction capacitances than in processes with < 0.5 \mu m feature sizes, by opening holes in the PD region.

III. PD LATERAL COLLECTION IMPROVEMENT

The photosensitive element in APS pixels, the PD, works in charge integration-mode where pixels are accessed at the end of a time interval called the integration period. When it is accessed, PD is read and then cleared for next scene integration. Fig. 3 shows the cross section of a PN-junction PD formed in a CMOS process; the PD is reverse-biased and formed by using the shallow N+ doped, drain–source diffusion of an nMOS device. A bias voltage applied to the N+ region forms a depletion region around the metallurgical PN-junction, which is free of any charge because of the electrical field. Any electron–hole pairs generated in this region see the electrical field as shown in the AA' cross section view of the PD in Fig. 3. Electrons slide in the opposite direction of the electric field (toward the N+ region), while holes slide toward the P-region; electrons are collected in a charge pocket in the N+ region, while holes are recombined. This type of PD has been widely used in CMOS and early CCD-type image sensors as a photo conversion and collection element.

There are two dark-current issues associated with using the standard N+ diffusion layer of an nMOS transistor as a photosensitive element. First is the dark current induced by stress centers around the N+ diffusion [9]; these stress centers are formed during the field oxide (FOX) formation in standard sub-micrometer CMOS processes. The second issue is the surface-related dark current generated from the work function difference between the N+ diffusion surface and overlaying isolation oxide layer. This second dark current causes surface recombination centers and defects. Both localities and stress centers absorb photo-generated electron–hole pairs close to the sur-
face, resulting in quantum loss at shorter wavelengths. As a result, silicon PDs show less sensitivity in the blue region of the spectrum (<400 nm), adding the very short absorption depth of these photons. Most blue photons are collected through lateral diffusion of the carriers generated on, or in the vicinity of, a PD peripheral—known as peripheral photoresponse or lateral photocurrent [13]. Thus, increasing lateral collection centers or peripheral length of a PD potentially improves collection efficiency for short-wavelength photons [14], [15] as it is depicted in Fig. 4. This method was adopted for UV PD devices in P-well CMOS processes [16].
Fig. 6. Test pixels with circular openings. (a) c17. (b) c14. (c) c11. (d) c7.

Fig. 7. Analog signal chain from pixel to chip output.

to shift column ASP contents sequentially to the global readout block. A shift-register type decoder was used in the column, too. Decoder control signals were generated in the timing generator block separately for frame operation. A pseudo-differential charge amplifier and sample-and-hold circuits were used in the global readout block. Chip outputs were in differential analog signals (SIG) and reset (RST). Signal analog-to-digital conversion used an analog-frame-grabber card.

A detailed schematic of the prototype imager’s analog signal chain is shown in Fig. 7, [10]. Each column contains a pMOS source follower, two sample-and-hold capacitors and a number of switches. A pMOS source follower was used for level shifting and signal amplification. Column signals were read during column time through single channel, pseudo-differential charge amplifiers and buffered for off-chip analog-to-digital conversion.

Fig. 8 shows a microphotograph of the prototype imager. The prototype was designed in 0.5-μm, 5-V 2P3M CMOS process, and different test pixel quadrants could be recognized on the pixel array with the naked eye. Table I provides specifications for the prototype imager.

Global charge amplifier gain was adjusted so that the gain-loss in pixel and column source followers balanced to achieve unity gain from pixel-to-chip output. Operating at 5 Mp/s readout speed, the prototype achieved a 30-frame per second (FPS) frame rate. A 5-V supply was used and the total power consumption of the chip was <200 mW. Noise floor of the readout channel was 850 μV.

VI. MEASUREMENT RESULTS AND DISCUSSIONS

Electrical and optical characteristics of circular-opening reference and test pixels measured under the same environmental and imaging conditions, [10].

A. Conversion Gain and Pixel Full-Well Capacity

Conversion gain and the full-well saturation voltage of the reference and test pixels were measured to determine pixel well capacity. Measurement results are shown in Fig. 9. Pixel well capacity increases with proper utilization of the PD peripheral junction, by using the holes on the PD diffusion region. Conversion gain of the pixel reduces with increased pixel capacitance, and the pixel full-well capacity increases.

It was observed that a linear correlation between total peripheral capacitance and pixel full-well capacity exist, because $C_A$ is almost equal to $C_P$ in the process used.
The area loss was compensated for by the peripheral increase, by a factor of 2.5. Because the radius of the opening was set to 0.8 μm, and the opening peripheral was \( p = 2\pi r \) 5.027 μm while the area was \( \alpha = \pi r^2 \) 2.01 μm². A factor of four could easily be achieved by choosing an opening radius of approximately 0.5 μm. However, reducing diameter results in depletion region overlap, and lowers peripheral capacitance and utilization.

**B. Quantum Efficiencies (QE)**

Quantum efficiencies (QE) of the reference (REF) and test pixels were measured by using a very stable light source, a monochromator, and a calibrated PD. Measurement was performed between 390 and 700 nm, with 10-nm steps. QE measurement results for reference (REF) and test pixels (c17, c14, c11) are shown in Fig. 10. In the figure, QE difference between the reference pixel and a test pixel with 17 openings (c17), normalized by reference QE, was also plotted. Spectral response improvement was observed with an increased number of openings on the PD. The most improvement was achieved at the shorter wavelengths and large number of openings, which is more visible in Fig. 11. Blue photons generated as electron–hole pairs close to the surface of the silicon were collected better laterally at close surroundings of the PD area. By adding circular openings these lateral collection areas were increased, which leads to a better QE response at shorter wavelengths. However, deep-penetrating photon collection probability did not increase as much as that of surface photons, giving less improvement in longer wavelengths.

**C. Dark Current**

Measured dark current for the reference pixel was 10.63 mV/s at room temperature, or 3155 e⁻/s with the measured conversion gain of 3.37 μV per electron. More dark current was observed from the test pixels with longer peripherals than the reference pixel, as shown in Fig. 12. Dark current, in terms of electrons per second, increases by approximately one-third of the reference dark electrons when the PD peripheral doubles (assuming the surface dark current effect was neglected).

In reality, measured dark current has two components, surface dark current and stress-center–related dark current. Surface dark current is related to the area of the PD, while stress-center-based dark current is related to the peripheral region. Opening a hole on a PD region reduces the surface contribution and increases the peripheral contribution on the total dark current. It is possible to determine the contribution of these two components of the dark current by designing fixed-area and varying-peripheral test pixels.

Dark current also increases noise floor effectively working against the gain achieved by PPMU method. In current design this contribution was not observed because the readout noise was larger than the dark current shot noise in low light condition.
TABLE II
KEY MEASURED PIXEL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Pixel Design</th>
<th>C17</th>
<th>C14</th>
<th>C11</th>
<th>C7</th>
<th>REF</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>PD Area</td>
<td>107.5</td>
<td>113.5</td>
<td>119.6</td>
<td>127.6</td>
<td>141.7</td>
<td>µm²</td>
</tr>
<tr>
<td>PD Peripheral</td>
<td>130.1</td>
<td>115.0</td>
<td>99.9</td>
<td>79.8</td>
<td>44.6</td>
<td>µm</td>
</tr>
<tr>
<td>Dark Current</td>
<td>6.31</td>
<td>5.29</td>
<td>4.84</td>
<td>4.25</td>
<td>3.19</td>
<td>Ke/µsec</td>
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<tr>
<td>Conversion Gain</td>
<td>2.80</td>
<td>2.95</td>
<td>3.02</td>
<td>3.19</td>
<td>3.37</td>
<td>eV/µV</td>
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<tr>
<td>Quantum Efficiency</td>
<td>26.22</td>
<td>25.24</td>
<td>25.26</td>
<td>24.58</td>
<td>23.41</td>
<td>% @ 390nm</td>
</tr>
<tr>
<td></td>
<td>50.00</td>
<td>49.41</td>
<td>49.24</td>
<td>47.97</td>
<td>47.44</td>
<td>% @ 550nm</td>
</tr>
<tr>
<td></td>
<td>51.31</td>
<td>50.35</td>
<td>50.72</td>
<td>50.05</td>
<td>48.55</td>
<td>% @ peak</td>
</tr>
<tr>
<td>QE improvement</td>
<td>12.0</td>
<td>8.3</td>
<td>7.9</td>
<td>5.0</td>
<td>0.0</td>
<td>%QEREF @ 390nm</td>
</tr>
<tr>
<td></td>
<td>7.5</td>
<td>4.2</td>
<td>3.8</td>
<td>1.1</td>
<td>0.0</td>
<td>%QEREF @ 550nm</td>
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<tr>
<td>Sensitivity</td>
<td>2.02</td>
<td>2.09</td>
<td>2.13</td>
<td>2.27</td>
<td>2.44</td>
<td>Volt/Lux sec</td>
</tr>
<tr>
<td>Pixel Full-Well Depth</td>
<td>621.4</td>
<td>583.1</td>
<td>577.6</td>
<td>545.2</td>
<td>500.7</td>
<td>Ke-</td>
</tr>
<tr>
<td>Pixel Full-Well Improvement</td>
<td>22.1</td>
<td>14.6</td>
<td>13.5</td>
<td>7.2</td>
<td>0.0</td>
<td>%FWREF</td>
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<tr>
<td>Capacitance</td>
<td>57.1</td>
<td>54.2</td>
<td>53.1</td>
<td>50.3</td>
<td>47.5</td>
<td>F</td>
</tr>
</tbody>
</table>

Fig. 13. Measured sensitivity of the reference and test pixels.

Measured dynamic range was around 66 dB due to the higher readout channel noise.

Dark current electrons add up in pixel capacity, yet, their contribution is less that 0.5% of the full well capacity in worst case.

D. Sensitivity

Sensitivity of the test and reference pixels were measured with a very sharp green (550 nm ± 20 nm) bandpass filter at 175 ms integration time. Measurement results are shown in Fig. 13. Sensitivity’s correlation with pixel capacity was extracted by fixing the light wavelength, pixel fill factor, and integration time. It was observed that the higher the pixel capacity, the lower the sensitivity was, for an inverse correlation. A 20 percent increase in pixel capacity causes a 17 percent decrease in pixel sensitivity between reference and test pixels with 17 openings, as shown in Fig. 13.

VII. CONCLUSION

PD-type CMOS APS pixels’ quantum efficiency was improved by opening number of circular holes on the PD diffusion area of a prototype imager. A method called PPUM was developed to accommodate pixel performance improvement in a fixed size pixel. Utilizing PPUM, four test pixels with 7, 11, 14, and 17 circular openings, and a reference pixel (REF), were designed, fabricated, and tested in a prototype APS imager made with a 0.5-µm, 5 V, 2P3M CMOS process. Measured pixel characteristics are summarized in Table II.

From the test pixels, we found that PPUM could be used to improve the quantum efficiency and full-well capacity, at the expense of increased dark current and noise level. Compared with the reference pixel (REF), total pixel QE improvement at 390 nm was 12 percent for 17 circular openings. Pixel full-well capacity improved 22 percent in the same pixel size, and dark current doubled between reference and C17 pixels.

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REFERENCES


Suat Utku Ay (S’96, M’02) received the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles (USC), CA, in 1997 and 2005, respectively. His Ph.D. thesis involved in designing large format scientific CMOS image sensors for space applications. He was Research And Teaching Assistant at USC from 1996 until 1998, where he worked on low-voltage, low-power, mixed-signal integrated circuits for implantable biomedical devices. In 1997, he joined Photobit Corporation in where he involved in number of innovative CMOS image sensor design projects for government and private customers. Between November 2001 and July 2007, he was working for Micron Technology Inc., Micron Imaging Group, Pasadena, CA. He joined academic faculty of Electrical and Computer Engineering Department, University of Idaho, Moscow, in August 2007 as an Assistant Professor. His research activities focused on CMOS image sensors and pixels, imaging devices and pixel modeling, imager and sensor readout circuit design, and low-power, low-voltage mixed-signal integrated circuit and system design.